ABSTRACT OF THE DISCLOSURE

The semiconductor wafer containment device or wafer box includes a base with a planar floor and a double concentric cylindrical wall structure arising therefrom. The double concentric cylindrical wall structure includes slots through which latch elements pivot radially. The latch elements include an inward padded spacer element. The latch elements pivot between an outward position wherein the padded spacer elements are relatively away from the wafer containment space and an inward upright position wherein the padded spacer elements impinge into the wafer containment space and are urged against the semiconductor wafers therein. Ramps on the lid capture the latch elements in the outward position and urge the latch elements to pivot to the inward upright position and be detent engaged in this position by slots formed on the lid.